



TPS7H1101-SP 1.5-V to 7-V Input, 3-A, Radiation-Hardened Ultra-Low Dropout (LDO) Regulator

1 Features

- [5962R13202](#):
 - Radiation Hardness Assurance (RHA) up to TID 100 krad (Si)
 - Total Ionizing Dose 100 krad (Si)
 - ELDRS-Free 100 krad (Si)
 - Dose Rate 10 mRAD(Si)/s
 - Single Event Latchup (SEL) Immune to LET = 85 MeV-cm²/mg
 - SEB and SEGR Immune to LET = 85 MeV-cm²/mg
 - SET/SEFI Onset Threshold >40 MeV-cm²/mg, See [Radiation Report](#) for Details
 - Specifically Designed to Always Upset Low to Avoid Damage to Critical Downstream Component
 - SET/SEFI Cross-Section Plot, See [Radiation Report](#) for Details
- Ultra-Low V_{IN} Range: 1.5 to 7 V
- 3-A Maximum Output Current
- Current Share/Parallel Operation to Provide up to 6-A Output Current
- Stable With Ceramic Output Capacitor
- ±1.25% Accuracy over Line, Load, and Temperature
- Programmable Soft-Start Through External Capacitor
- Input Enable and Power-Good Output for Power Sequencing
- Ultra-Low Dropout LDO Voltage: 62 mV at 1 A (25°C), V_{OUT} = 1.8 V
- Low Noise: 20.33 μVRMS V_{IN} = 2 V, V_{OUT} = 1.8 V at 3 A
- PSRR: Over 45 dB at 1 kHz
- Excellent Load/Line Transient Response
- Foldback Current Limit
- See the [Tools & Software](#) Tab
- Thermally-Enhanced CFP Package (0.6°C/W R_{θJC})

2 Applications

- Space Satellite Point of Load Supply for FPGAs, Microcontrollers, ASICs, and Data Converters
- Space Satellite Payloads
- Radiation-Hardened Low-Noise Linear Regulator Power Supply for RF, VCOs, Receivers, and Amplifiers
- Clean Analog Supply Requirements
- Available in Military (–55°C to 125°C) Temperature Range
- Engineering Evaluation (/EM) Samples are Available⁽¹⁾

3 Description

The TPS7H1101-SP is a radiation-hardened LDO linear regulator that uses a PMOS pass element configuration. It operates under a wide range of input voltage, from 1.5 to 7 V while offering excellent PSRR. The TPS7H1101-SP features a precise and programmable foldback current limit implementation with a very-wide adjustment range. To support the complex power requirements of FPGAs, DSPs, or microcontrollers, the TPS7H1101-SP provides enable on and off functionality, programmable SoftStart, current sharing capability, and a PowerGood open-drain output.

Device Information⁽²⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7H1101-SP	CFP (16)	11.00 mm × 9.60 mm

(1) These units are intended for engineering evaluation only. They are processed to a noncompliant flow (that is, no burn-in, and so forth) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

(2) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

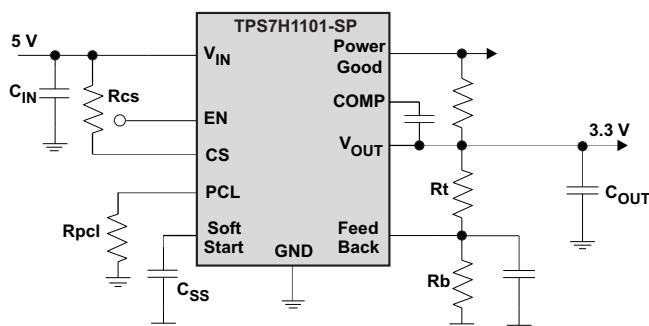


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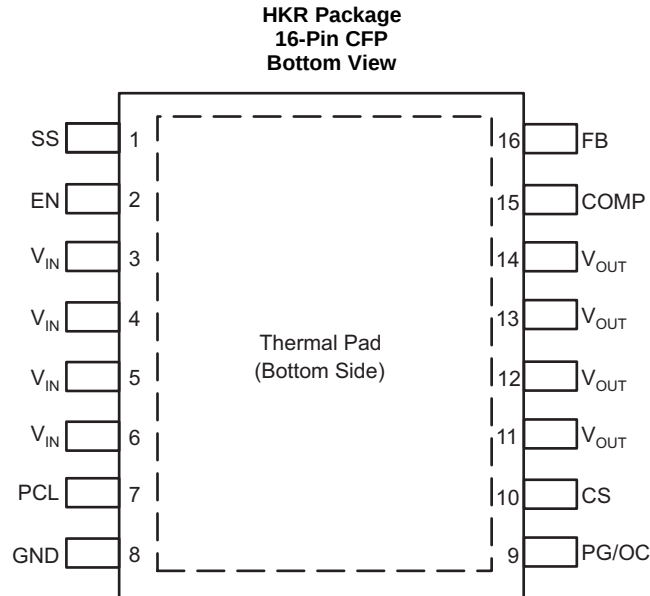
4 Revision History

DATE	REVISION	NOTES
January 2016	*	Initial release. • Created separate data sheet for this part number • Corrected the thermal values for $R_{\theta JB}$ • Corrected y-axis scale for Figure 16 • Removed the ψ_{JT} thermal metric

5 Description (continued)

The TPS7H1101-SP is available in a thermally-enhanced 16-pin ceramic flatpack package (CFP).

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SS	1		Soft-Start terminal. Connecting an external capacitor slows down the output voltage ramp rate after enable event. The Soft-Start terminal can be used to disable the device as described in Soft-Start .
EN	2		Enable terminal. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device; V_{IN} voltage must be greater than 3.5 V. For $V_{IN} < 3.5$ V, enable terminal cannot be used to disable the device. TI recommends to connect the enable terminal to V_{IN} .
V_{IN}	3		Unregulated supply voltage. TI recommends to connect an input capacitor as a good analog circuit practice.
	4		
	5		
	6		
PCL	7		Programmable current limit. A resistor to GND sets the overcurrent limit activation point. The range of resistor that can be used on the PCL terminal to GND is 8.2 to 160 k Ω .
GND	8	—	Ground/thermal pad ⁽¹⁾
PG/OC	9		PowerGood terminal. PG is an open-drain output to indicate the output voltage reaches 90% of target. PG terminal is also used as indicator when an overcurrent condition is activated.
CS	10		Current sense terminal. Resistor connected from CS to V_{IN} . CS terminal indicates voltage proportional to output current. CS terminal low: Foldback current limit disabled CS terminal high: Foldback current limit enabled
V_{OUT}	11		Regulated output
	12		
	13		
	14		
COMP	15		Output of error amplifier
FB	16		The output voltage feedback input through voltage dividers. See Adjustable Output Voltage (Feedback Circuit) .

(1) Thermal pad must be connected to GND

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Input voltage	V _{IN} , PG	−0.3	7.5	V
	FB, COMP, PCL, CS, EN	−0.3	V _{IN} + 0.3	V
Output voltage	V _{OUT} , SS	−0.3	V _{IN}	V
Peak output current		Internally limited		A
PG terminal sink current		0.001	5	mA
Maximum operating junction temperature, T _J		−55	150	°C
Storage temperature, T _{stg}		−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T _J	Operating junction temperature	−55		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾⁽²⁾		TPS7H1101-SP	UNIT
		HKR (CFP)	
		16 PINS	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	0.6	°C/W

- (1) Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.
(2) Maximum power dissipation may be limited by overcurrent protection.

7.5 Electrical Characteristics

$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT(target)} = V_{IN} - 0.35\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.1\text{ V}$, $C_{OUT} = 22\text{ }\mu\text{F}$, PG terminal pulled up to V_{IN} with $50\text{ k}\Omega$, over operating temperature range ($T_J = -55^\circ\text{C}$ to 125°C), unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} Input voltage range		1.5		7	V
V_{FB} Feedback terminal voltage ⁽¹⁾⁽¹⁾	$0\text{ A} \leq I_{OUT} \leq 3\text{ A}$, $1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$	0.594	0.605	0.616	V
V_{OUT} Output voltage range		0.8		$V_{IN} - 0.35$	V
Output voltage accuracy ⁽¹⁾	$0\text{ A} \leq I_{OUT} \leq 3\text{ A}$, $1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 0.8\text{ V}, 1.2\text{ V}, 1.8\text{ V}, 6.65\text{ V}$	-2%		2%	
$\Delta V_{OUT}\% / \Delta V_{IN}$ Line regulation	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$	-0.07	0.01	0.07	%/V
$\Delta V_{OUT}\% / \Delta I_{OUT}$ Load regulation	$0.8\text{ V} \leq V_{OUT} \leq 6.65\text{ V}$, $0 \leq I_{Load} \leq 3\text{ A}$		0.08		%/A
ΔV_I DC input line regulation	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 0.8\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = -55^\circ\text{C}$ ⁽²⁾		0.5	3	mV
	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 0.8\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ ⁽²⁾		0.2	0.6	
	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 0.8\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = 125^\circ\text{C}$ ⁽²⁾		0.2	1.0	
	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = -55^\circ\text{C}$ ⁽²⁾		0.5	3.0	
	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ ⁽²⁾		0.2	0.6	
	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = 125^\circ\text{C}$ ⁽²⁾		0.2	1.0	
	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = -55^\circ\text{C}$ ⁽²⁾		0.5	3.0	
	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ ⁽²⁾		0.2	0.6	
	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 10\text{ mA}$, $T_J = 125^\circ\text{C}$ ⁽²⁾		0.2	1.0	

(1) The output voltage accuracy of condition at $I_{OUT} = 2\text{ A}$ and $I_{OUT} = 3\text{ A}$ is specified by characterization, but not production tested.

(2) Line and load regulations done under pulse condition for $t < 10\text{ ms}$.

Electrical Characteristics (continued)

1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT(target)} = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 μF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV _O	DC output load regulation ⁽³⁾	V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 1 A, T _J = –55°C ⁽²⁾		0.4	1.0	mV
		V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 1 A, T _J = 25°C ⁽²⁾		0.6	1.1	
		V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 1 A, T _J = 125°C ⁽²⁾		0.8	1.3	
		V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 2 A, T _J = –55°C ⁽²⁾		0.8	1.8	
		V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 2 A, T _J = 25°C ⁽²⁾		1.3	1.8	
		V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 2 A, T _J = 125°C ⁽²⁾		1.6	2.4	
		V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 3 A, T _J = –55°C ⁽²⁾		1.1	1.9	
		V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 3 A, T _J = 25°C ⁽²⁾		1.9	2.6	
		V _{OUT} = 0.8 V, 0 ≤ I _{Load} ≤ 3 A, T _J = 125°C ⁽²⁾		2.5	3.4	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 1 A, T _J = –55°C ⁽²⁾		0.3	1.2	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 1 A, T _J = 25°C ⁽²⁾		0.5	1.3	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 1 A, T _J = 125°C ⁽²⁾		0.6	1.3	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 2 A, T _J = –55°C ⁽²⁾		0.8	1.6	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 2 A, T _J = 25°C ⁽²⁾		1.1	2.1	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 2 A, T _J = 125°C ⁽²⁾		1.5	2.1	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 3 A, T _J = –55°C ⁽²⁾		1.0	1.7	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 3 A, T _J = 25°C ⁽²⁾		1.1	2.4	
		V _{OUT} = 1.2 V, 0 ≤ I _{Load} ≤ 3 A, T _J = 125°C ⁽²⁾		2.2	3.5	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 1 A, T _J = –55°C ⁽²⁾		0.1	0.9	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 1 A, T _J = 25°C ⁽²⁾		0.3	0.9	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 1 A, T _J = 125°C ⁽²⁾		0.4	1.2	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 2 A, T _J = –55°C ⁽²⁾		1.4	2.4	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 2 A, T _J = 25°C ⁽²⁾		0.7	1.4	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 2 A, T _J = 125°C ⁽²⁾		0.6	1.9	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 3 A, T _J = –55°C ⁽²⁾		2.5	3.9	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 3 A, T _J = 25°C ⁽²⁾		1.2	2.1	
		V _{OUT} = 1.8 V, 0 ≤ I _{Load} ≤ 3 A, T _J = 125°C ⁽²⁾		1.2	2.5	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 1 A, T _J = –55°C ⁽²⁾		1.5	2.9	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 1 A, T _J = 25°C ⁽²⁾		0.4	2.6	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 1 A, T _J = 125°C ⁽²⁾		2.8	3.5	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 2 A, T _J = –55°C ⁽²⁾		3.5	5.9	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 2 A, T _J = 25°C ⁽²⁾		1.1	4.7	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 2 A, T _J = 125°C ⁽²⁾		5.8	8.0	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 3 A, T _J = –55°C ⁽²⁾		5.6	9.3	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 3 A, T _J = 25°C ⁽²⁾		3.7	8.0	
		V _{OUT} = 6.65 V, 0 ≤ I _{Load} ≤ 3 A, T _J = 125°C ⁽²⁾		13.0	25	
V _{DO}	Worst case dropout voltage ⁽³⁾	I _{OUT} = 3 A, V _{OUT} = 1.3 V, V _{IN} = V _{OUT} + V _{DO}		210	335	mV
	Dropout voltage ⁽³⁾	I _{OUT} = 3 A, V _{OUT} = 1.8 V, V _{IN} = V _{OUT} + V _{DO}		196		
I _{CL}	Programmable output current limit range	V _{IN} = 1.5 V, V _{OUT} = 1.2 V, PCL resistance = 47 kΩ	500		750	mA
		V _{IN} = 1.5 V, V _{OUT} = 1.2 V, PCL resistance varies	200		3500 ⁽⁴⁾	mA
V _{CS}	Operating voltage range at CS		0.3		V _{IN}	V

(3) The parameter is specified to the limit in characterization, but not production tested.

(4) The maximum limit of the I_{CL} parameter is specified to the limit in characterization, but not production tested.

Electrical Characteristics (continued)

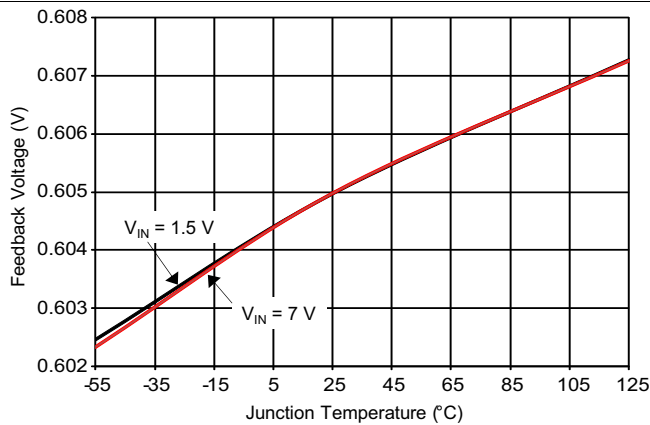
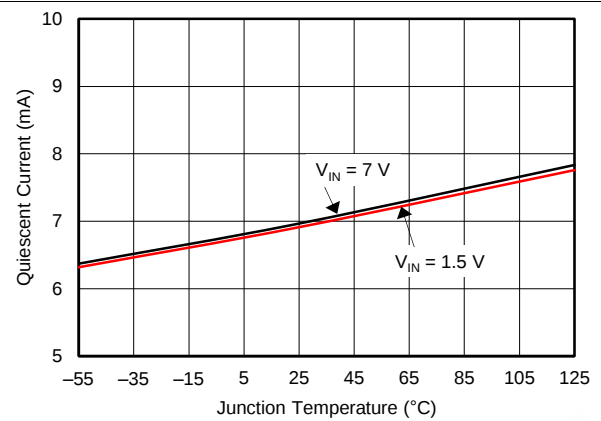
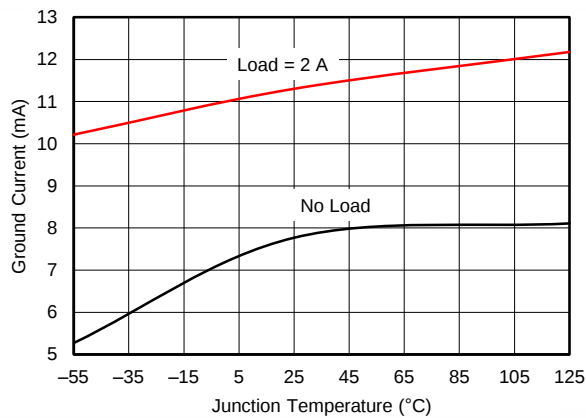
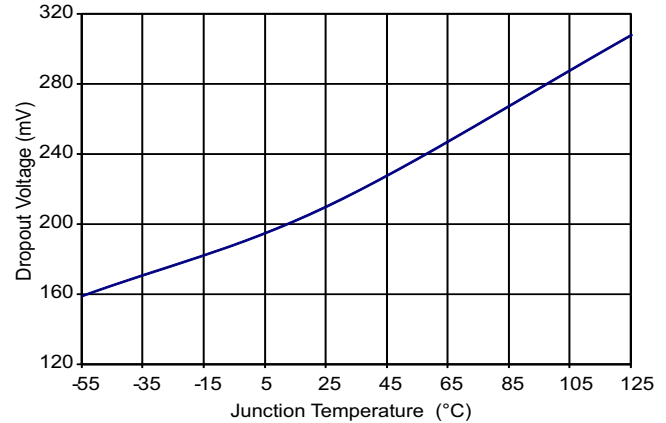
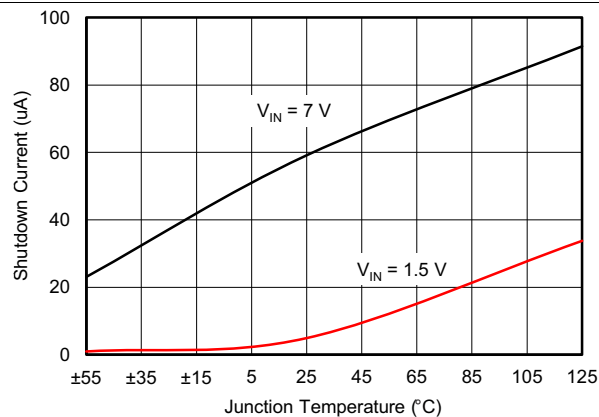
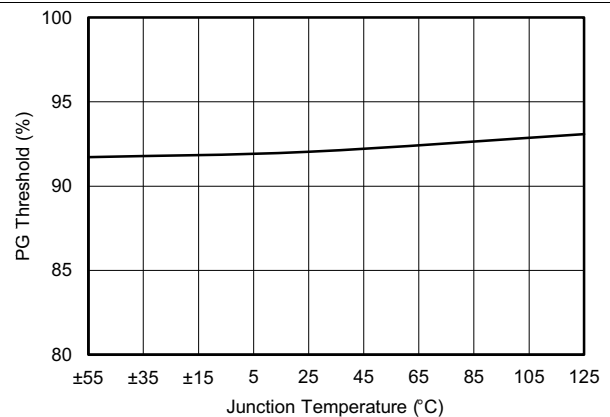
$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, $V_{OUT(target)} = V_{IN} - 0.35\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.1\text{ V}$, $C_{OUT} = 22\text{ }\mu\text{F}$, PG terminal pulled up to V_{IN} with $50\text{ k}\Omega$, over operating temperature range ($T_J = -55^\circ\text{C}$ to 125°C), unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CSR	Current sense ratio	I_{LOAD} / I_{CS} , $V_{IN} = 2.3\text{ V}$, $V_{OUT} = 1.9\text{ V}$	47500	47394	56000	
I_{GND}	GND terminal current	$V_{IN} = 1.5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 2\text{ A}$		10	16	mA
I_Q	Quiescent current (no load)	$V_{IN} = V_{OUT} + 0.5\text{ V}$, $I_{OUT} = 0\text{ A}$		7	10	mA
I_{SHDN}	Shutdown current	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$		26	230	μA
		$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$, Post 100 kRads (si), $T_J = 25^\circ\text{C}^{(5)}$			1400	μA
I_{SNS} , I_{FB}	FB/SNS terminal current	$V_{IN} = 7\text{ V}$, $V_{OUT} = 6.65\text{ V}$		1	5	nA
I_{EN}	EN terminal input current	$V_{IN} = 7\text{ V}$, $V_{EN} = 7\text{ V}$, $V_{OUT} = 6.65\text{ V}$		20	150	nA
V_{ILEN}	EN terminal input low (disable)	$3.5\text{ V} < V_{IN} < 7\text{ V}$		$0.30 \times V_{IN}$		V
V_{IHEN}	EN terminal input high (enable)	$3.5\text{ V} < V_{IN} < 7\text{ V}$		$0.75 \times V_{IN}$		V
Eprop Dly	Enable terminal propagation delay	$V_{IN} = 2.2\text{ V}$, EN rise to $I_{OUTrise}$		650	1000	μs
T_{EN}	Enable terminal turn-on delay	$V_{IN} = 2.2\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{LOAD} = 1\text{ A}$, $C_{OUT} = 220\text{ }\mu\text{F}$, $C_{SS} = 2\text{ nF}$		1.4	1.6	ms
V_{THPG}	PG threshold	No load, $0.8\text{ V} \leq V_{OUT} \leq 6.65\text{ V}$	86	90%		
$V_{THPGHYS}$	PG hysteresis	$1.5\text{ V} \leq V_{IN} \leq 7\text{ V}$		2%		
V_{OLPG}	PG terminal output low	$I_{PG} = 0$ to -1 mA		120	300	mV
I_{LKPG}	PG terminal leakage current	$V_{OUT} > V_{THPG}$, $V_{PG} = 1.2\text{ V}$		0.2	1.5	μA
		$V_{OUT} > V_{THPG}$, $V_{PG} = 7\text{ V}$		0.5	2.5	μA
I_{SS}	SS terminal charge current	$V_{IN} = 1.5$ to 7 V		2.5	3.5	μA
I_{SSdisb}	SS terminal disable current	$V_{IN} = 1.5$ to 7 V		5	10	μA
V_{SS}	SS terminal voltage (device enabled) ⁽⁶⁾	$V_{IN} = 1.5$ to 7 V			1.232	V
V_{SSdisb}	SS terminal low-level input voltage to disable device	$V_{IN} = 1.5$ to 7 V			0.4	V
PSRR	Power-supply rejection ratio	$V_{IN} = 2.5\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $C_{OUT} = 220\text{ }\mu\text{F}$	1 kHz	48		dB
			100 kHz	25		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, $I_{OUT} = 3\text{ A}$, $V_{IN} = 2\text{ V}$, $V_{OUT} = 1.8\text{ V}$		20.33		μV_{RMS}
TSD	Thermal shutdown temperature			185		$^\circ\text{C}$
T_J	Operating junction temperature		-55		125	$^\circ\text{C}$

(5) This maximum limit applies to SMD 5962R13202 post 100 kRads (Si) test at 25°C .

(6) Any external pullup voltage should not exceed 1.188 V.

7.6 Typical Characteristics


Figure 1. Feedback Voltage vs Temperature

Figure 2. Quiescent Current vs Temperature

Figure 3. Ground Current vs Temperature

Figure 4. Dropout Voltage vs Temperature

Figure 5. Shutdown Current vs Temperature

Figure 6. PU Threshold vs Temperature

8 Detailed Description

8.1 Overview

The TPS7H1101-SP is 3-A, 1.5- to 7-V LDO linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high thermal performance in a 16-pin ceramic flatpack package (HKR).

A number of features are incorporated in the design to provide high reliability and system flexibility. Current foldback, overload, current limit, and thermal protection are incorporated in the design to make it viable for harsh environments.

A resistor connected from the current sense (CS) terminal to VIN indicates voltage proportional to the output current. When CS is held high, foldback current limit is enabled. Shorting CS low disables the foldback current limit.

A resistor connected from the programmable current limit (PCL) terminal to ground sets the over current limit activation point. When overcurrent limit activation point is reached, it results in LDO going into current foldback mode. Output current is reduced to approximately 50% of the current limit set point.

TPS7H1101-SP incorporates thermal protection, which disables the output when the junction temperature rises approximately 185°C, allowing the device to cool. Depending on the power dissipation, thermal resistance, and ambient temperature, the thermal protection turns on. Cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The device also has a current sense monitoring feature. A resistor connected from the CS terminal to VIN indicates voltage proportional to the output load current. [PCL](#) provides a detailed description of this feature.

To provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in [Figure 8. Current Sharing](#) provides detailed parallel operation information.

An enable feature is incorporated in the design allowing the user to enable or disable the LDO. Power Good, an open-drain connection, indicates the status of the output voltage. These provide the customers system flexibility in monitoring and controlling the LDO operation. When using the Enable function, V_{IN} voltage must be >3.5 V. For V_{IN} from 1.5 to 7 V, TPS7H1101-SP can be disabled using the Soft-Start (SS) terminal as described in [Enable/Disable](#).

8.2 Functional Block Diagrams

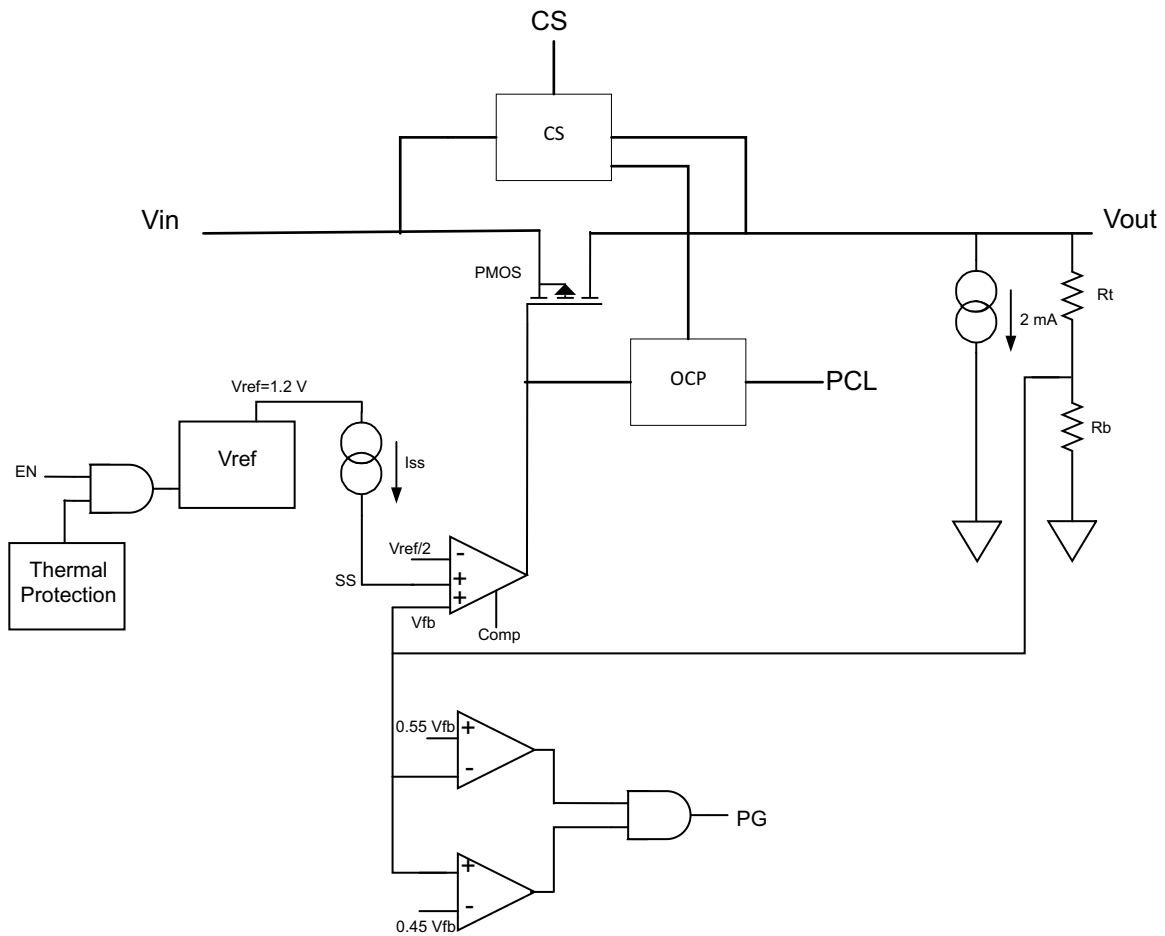


Figure 7. Block Diagram

Functional Block Diagrams (continued)

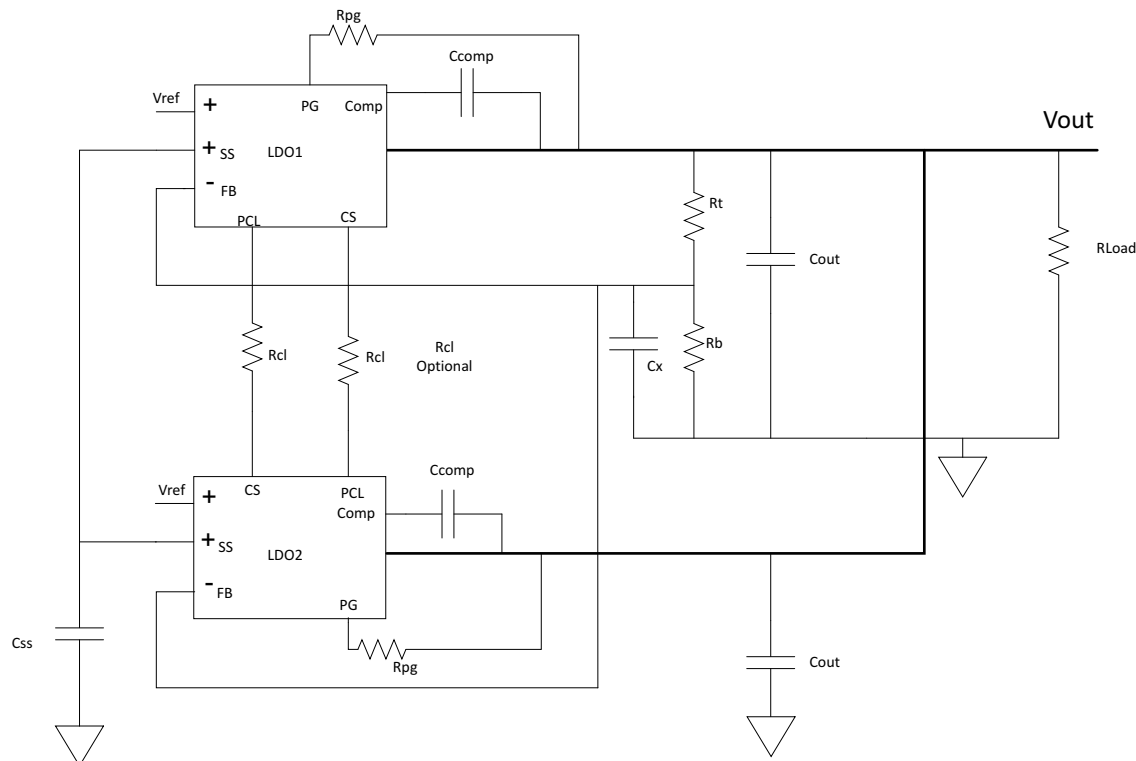


Figure 8. Block Diagram (Parallel Operation)

8.3 Feature Description

8.3.1 Soft-Start

Connecting a capacitor on the CS terminal to GND (C_{SS}) slows down the output voltage ramp rate. The soft-start capacitor charges up to 1.2 V.

$$C_{SS} = \frac{t_{SS} \cdot I_{SS}}{V_{FB}}$$

where

- t_{SS} = Soft-start time
- I_{SS} = 2.5 μ A
- $V_{FB} = V_{REF} / 2 = 0.605$ V

(1)

8.3.2 Power Good (PG)

Power Good terminal (9) is an open-drain connection and can be used to sequence multiple LDOs. [Figure 9](#) shows typical connection. As shown, maximum voltage at PG terminal must be limited to <1.2 V in order not to forward bias the internal MOSFET diode of PMOS current mirror circuitry.

Feature Description (continued)

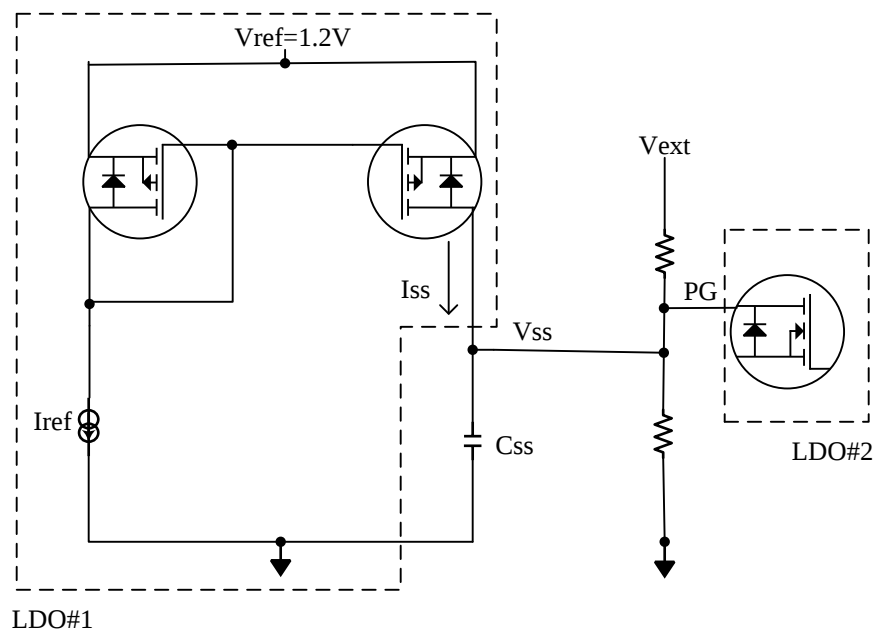


Figure 9. Sequencing LDO#1 by Power Good Signal of LDO#2

NOTE

For PSpice models, WEBENCH, and mini-POL reference design, see the *Tools & Software* tab.

1. PSpice average model (stability – bode plot)
2. PSpice transient model (switching waveforms)
3. WEBENCH design tool www.ti.com/product/TPS7H1101-SP/toolssoftware

8.4 Device Functional Modes

8.4.1 Enable/Disable

For V_{IN} from 1.5 to 7 V, TPS7H1101-SP can be disabled using the SS terminal. The minimum Soft-Start pulldown current is 10 μA , with soft-start to ground voltage of 400 mV or lower. External voltage applied to the SS terminal must be limited to 1.2-V maximum. Removing the logic-low condition on Soft-Start enables the device allowing the Soft-Start capacitor to get charged by the internal current source. Alternatively, for $V_{IN} > 3.5$ V, the device can be disabled by pulling the enable terminal to logic low. In all other cases, the enable terminal should be connected to V_{IN} .

Device Functional Modes (continued)

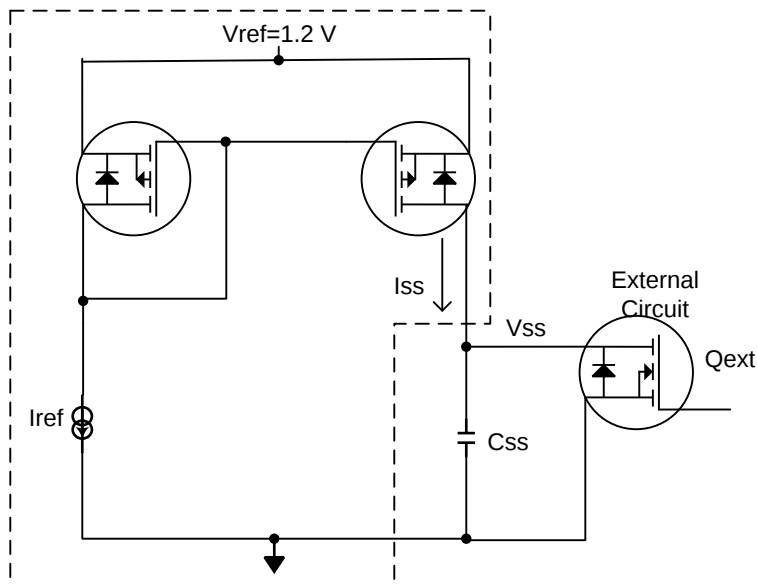


Figure 10. Enable/Disable

The circuit shown in [Figure 10](#) highlights the SS terminal 1 along with block diagram of internal circuitry. Circuitry in dashed outline is internal to the IC composed of PMOSFET current mirror. The PMOS current mirror sources current from the positive supply and external circuitry composed of Q_{ext} is used to sink current from SS terminal 1. As highlighted in the [Electrical Characteristics](#) table – typical $I_{SS} = 2.5 \mu A$ and max $I_{SS} = 3.5 \mu A$ for TPS7H1101-SP. If I_{SS} current is exceeded, such as sinking higher current in excess of max I_{SS} , this disables the LDO.

See the [Electrical Characteristics](#) table for the external sink current from SS terminal necessary to disable the IC. Exceeding maximum external sink current does not damage the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This TPS7H1101-SP family of LDO linear regulators, with output current capability up to 3 A are targeted for harsh environment applications. This family of regulators has various features such as low dropout, soft start, output current foldback, high-side current sensing (where sensing voltage at CS pin provides voltage proportional to output current), and current sharing. Thus, multiple LDOs can be daisy chained to provide higher output current for the demanding applications.

9.1.1 Stability

Conventional Bode plots are a standard approach in assessing stability as shown in Figure 11. This approach requires that we have a single feedback path where ac signal is injected across typically 50-Ω resistor and measurements are done on either side of the 50-Ω resistor. Thus gain and phase plots can be generated. Crossover frequency f_C is defined as the frequency where the magnitude of the loop gain is unity and phase margin is evaluated at the crossover frequency f_C .

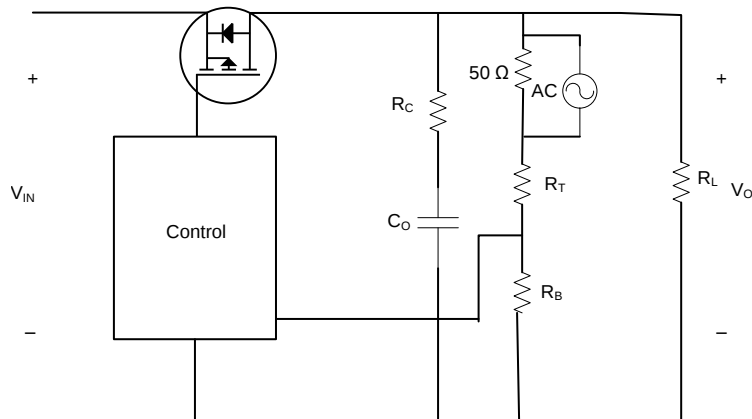


Figure 11. Conventional Bode Plot

However there are conditions where one does not have access to the feedback loop as all the feedback network and compensations are integrated in the package. This is evident with increased integration, thus only access point one has is the output terminal of the device.

There are other situations where one can have multiple feedback loops, an inner fast loop and an outer feedback loop. Inner fast loop helps to improve the loop response and thus provides high crossover frequency f_C and improved transient response. Crossover frequency f_C is defined as the frequency where the magnitude of the loop gain is unity.

When we have multiple feedback loops, conventional bode plot approach can not be used. One has to assess stability based upon measuring output impedance measurements.

With the addition of negative feedback, output impedance Z_{out} close loop (Z_{out_CL}) is reduced by $T(s)$ open loop gain as shown in Equation 2.

$$Z_{out_CL} = \frac{Z_{out}}{1 + T(s)} \quad (2)$$

Group delay T_g is the rate of change of phase with respect to frequency. Q of the circuit relates group delay and phase margin per Equation 3.

Application Information (continued)

$$T_g = d\phi \times d\omega \quad (3)$$

See reference [4].

$$Q = T_g \times \text{Frequency} \times \pi \quad (4)$$

See reference [4].

$$Q = \frac{\sqrt{\cos\phi_m}}{\sin\phi_m} \quad (5)$$

See reference [1].

$$\phi_m = \tan^{-1} \times \sqrt{\frac{1 + \sqrt{1 + 4 \times Q^4}}{2 \times Q^4}} \quad (6)$$

See reference [1].

Thus using the approach of assessing stability through measuring output impedance is a viable approach. One can validate the results by applying step load to the output and see the response. For TPS7H1101- SP, the designer will see it has crossover frequency of approximately 300 kHz with phase margin of 58° using the recommended output capacitance of 220-μF tantalum capacitor on the output.

9.2 Typical Application

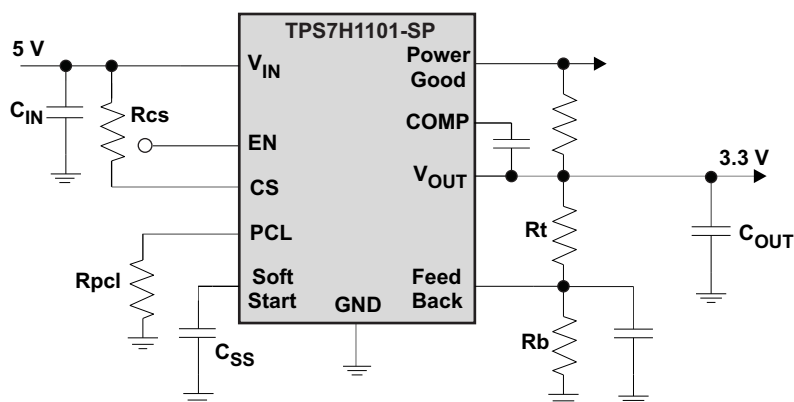


Figure 12. Typical Application Circuit

9.2.1 Design Requirements

Table 1 shows the design parameters.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage	1.5 to 7 V
Output voltage	User programmable
Output current	3-A max

9.2.2 Detailed Design Procedure

9.2.2.1 Adjustable Output Voltage (Feedback Circuit)

The output voltage of the TPS7H1101-SP can be set to a user-programmable level between 0.8 and 6.65 V. Achieve this by using a resistor divider connected between V_{OUT} , FB, and GND terminals. R_{TOP} connected between V_{OUT} and V_{FB} , and R_{BOTTOM} connected between V_{FB} and GND.

Use Equation 7 to determine V_{OUT} .

$$V_{OUT} = \frac{(R_{TOP} + R_{BOTTOM}) \cdot V_{FB}}{R_{BOTTOM}}$$

where

- $V_{FB} = 0.605 \text{ V}$ (7)

Table 2. Resistor Values for Typical Voltages

V_{OUT}	R_{TOP}	R_{BOTTOM}
0.8 V	10 k Ω	30.1 k Ω
1 V	10 k Ω	15 k Ω
1.2 V	10 k Ω	10 k Ω
1.5 V	15 k Ω	10 k Ω
1.8 V	20 k Ω	10 k Ω
2.5 V	32 k Ω	10.1 k Ω
3.3 V	45.9 k Ω	10.2 k Ω
4 V	59 k Ω	10.4 k Ω
5 V	77.7 k Ω	10.6 k Ω
5.5 V	78.7 k Ω	9.65 k Ω
6 V	78.7 k Ω	8.75 k Ω
6.5 V	78.7 k Ω	7.96 k Ω
6.6 V	79.6 k Ω	7.96 k Ω
6.7 V	78.7 k Ω	7.77 k Ω

9.2.2.2 PCL

PCL resistor, R_{pcl} , sets the overcurrent limit activation point and can be calculated per Equation 8.

$$R_{pcl} = (CSR \times V_{ref}) / (I_{CL} - 0.0403)$$

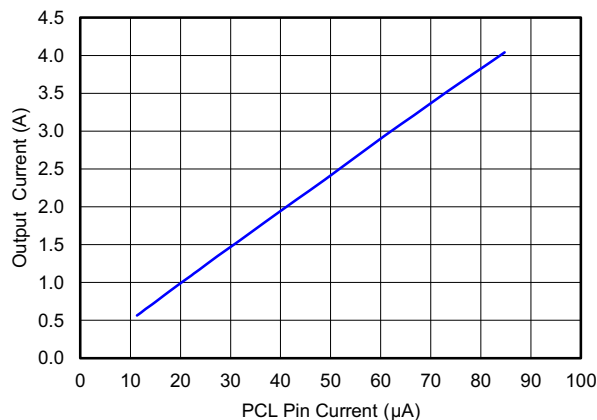
where

- $V_{ref} = 0.605 \text{ V}$
- I_{CL} = Programmable current limit (A)
- Current sense ratio (CSR) is the ratio of output load current to I_{CS} . The typical value of the CSR is 47394. (8)

Figure 13 shows the output load current (I_{OUT}) versus PCL terminal current (I_{CL})

A suitable resistor R_{pcl} must be chosen to ensure the CS terminal is within its operating range of 0.3 V to V_{IN} .

The maximum PCL is 3.5 A. The range of resistor that can be used on the PCL terminal to GND is 8.2 to 160 k Ω .



$$V_{IN} = 2.3 \text{ V} \quad V_{OUT} = 1.8 \text{ V} \quad y = 47394x + 0.0403$$

Figure 13. I_{OUT} (A) vs I_{PCL} (μA)

9.2.2.3 High-Side Current Sense

Figure 14 shows the cascode NMOS current mirror. V_{CS} must be in the range as specified in the [Electrical Characteristics](#) table. The following example shows the typical calculation of R_{CS} .

$$I_{CS} = \frac{I_{LOAD} + V_{offset}}{CSR} \quad (9)$$

$$R_{CS} = \frac{V_{IN} - V_{CS}}{I_{CS}}$$

where

- I_{LOAD} is the output load current.
- CSR is the current sense ratio.

When $V_{IN} = 2.3 \text{ V}$, select $V_{CS} = 2.05 \text{ V}$, $I_{LOAD} = 3 \text{ A}$, $CSR = 47394$, and $V_{offset} = 0.1899 \text{ A}$, then $I_{CS} = 67.306 \mu\text{A}$ and $R_{CS} = 3.714 \text{ k}\Omega$.

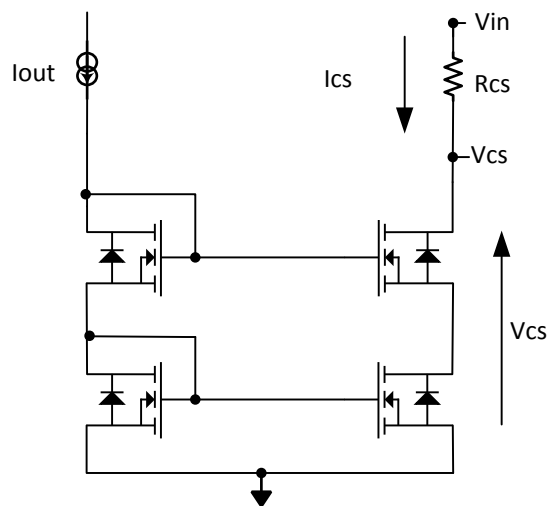


Figure 14. Cascode NMOS Current Mirror

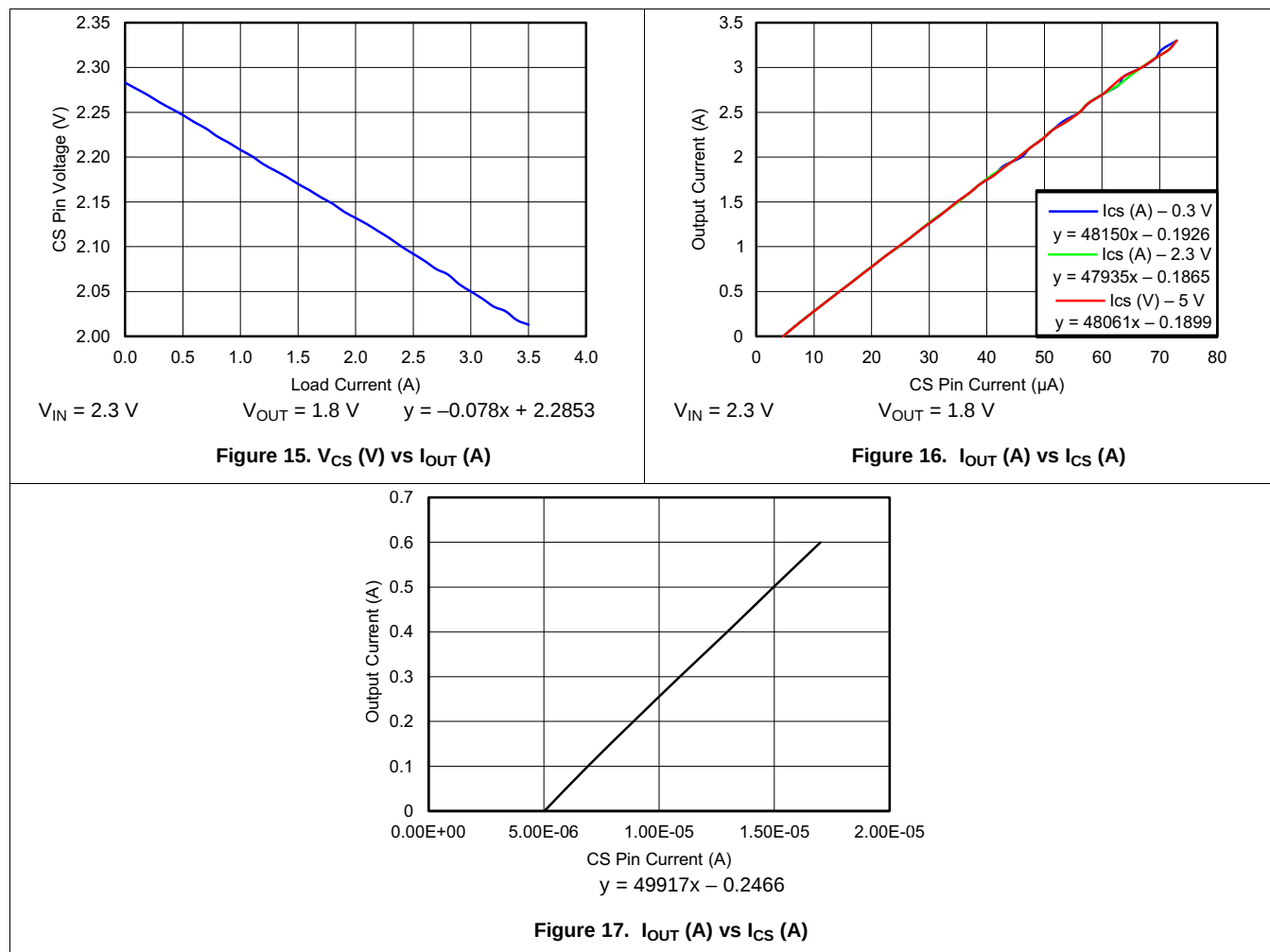
For TPS7H1101-SP, Figure 15 shows the typical curve V_{CS} vs I_{OUT} for $V_{IN} = 2.28 \text{ V}$ and $R_{CS} = 3.65 \text{ k}\Omega$. A resistor connected from the CS terminal to V_{IN} indicates voltage proportional to the output current.

Monitoring current in CS terminal (I_{CS} vs I_{OUT}) indicates the CSR between the main PMOSFET and the current sense MOSFET as shown in Figure 16.

For TPS7H1101-SP, monitoring the voltage at the CS terminal indicates voltage proportional to the output current. Figure 15 shows typical curve V_{CS} vs I_{OUT} for $V_{IN} = 2.28$ V and $R_{CS} = 3.65$ k Ω .

Monitoring current in CS terminal (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMOSFET and the current sense MOSFET as shown in Figure 16.

Figure 17 shows I_{OUT} vs I_{CS} when the voltage on CS terminal is varied from 0.3 to 7 V.



9.2.2.4 Current Foldback

1. The TPS7H1101-SP has a current foldback feature which can be enabled when the CS terminal is held high. Shorting CS low disables the foldback current limit.
2. With foldback current limit enabled, when current limit trip point is activated,
 - (a) Output voltage drops low
 - (b) Output current folds back to approximately 50% of the current limit trip point.
 This results in minimizing the power loss under fault conditions. Monitoring the voltage at the CS terminal indicates voltage proportional to the output current.

9.2.2.5 Transient Response

Figure 18, Figure 19, and Figure 20 indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Output voltage overshoot/undershoot

Channel 2: Step load in current

Channel 3: Input voltage

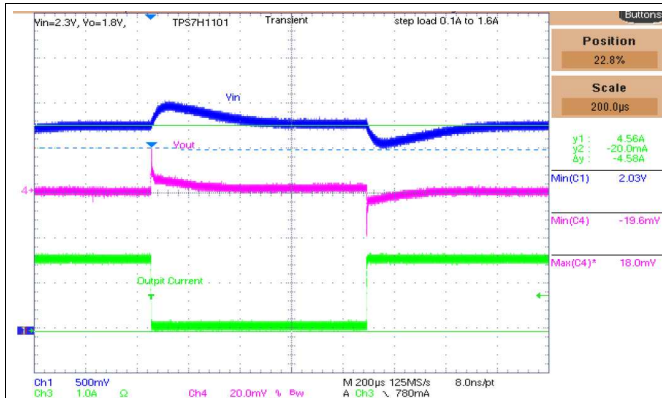


Figure 18. Load Transient Response: Step Load 0.1 to 1.6 A, $V_{IN} = 2.3$ V, $V_{OUT} = 1.8$ V

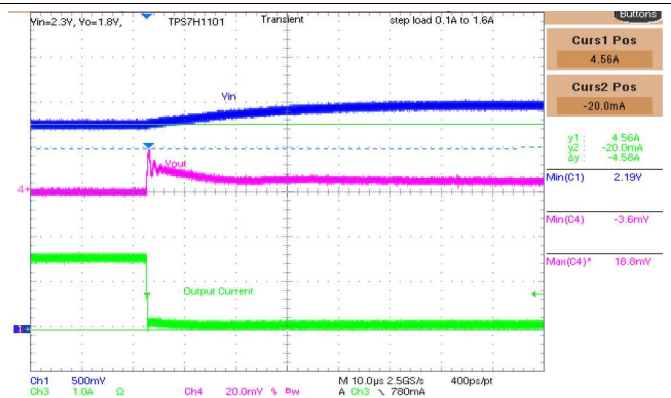


Figure 19. Expanded View Overshoot

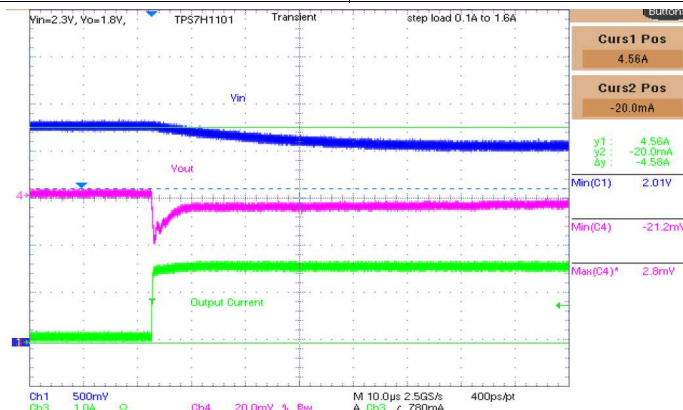


Figure 20. Expanded View Undershoot

9.2.2.6 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled as indicated in [Figure 8](#). In parallel mode, the CS terminal of LDO1 must be connected to the PCL terminal of LDO2 via a series resistor, R_{CL} , and CS terminal of LDO2 must be connected to PCL terminal of LDO1 via series resistor, R_{CL} . The typical value of R_{CL} in parallel operation is 3.75 k Ω for current limit >6 A. In parallel configuration, R_{CL} (resistor from PCL to GND) and R_{CS} (resistor from CS terminal to V_{IN}) must be left open (unpopulated). The R_{CL} value must be selected so that the operating condition of the CS terminal is maintained, as specified in the [Electrical Characteristics](#) table. The current from PCL through R_{CL} of LDO1 is determined by the output load current of LDO2 divided by the CSR. Hence, the voltage at CS terminal of the LDO1 is 0.605 V – ((output load current of LDO2 + 0.2458) / CSR $\times$ R_{CL}). Typical value of R_{CL} is 3.65 k Ω . This parallel configuration provides higher reliability (MTBF) for system needs due to reduced stress on the components, as the load current is shared between the two LDOs.

Alternately, it can also provide twice the output current to meet system needs. When using two LDOs in parallel operation for higher output load current, use POL TPS7H1101-SP as an input source.

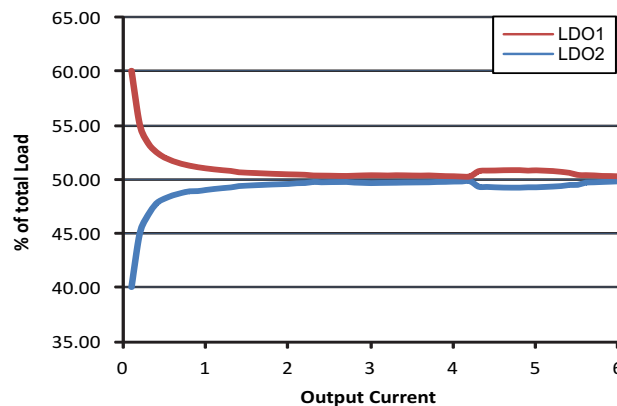


Figure 21. LDO Current Share

9.2.2.7 Compensation

Figure 22 shows a generic block diagram for TPS7H1101-SP LDO with external compensation components. LDO incorporates nested loops, thus providing the high gain necessary to meet design performance.

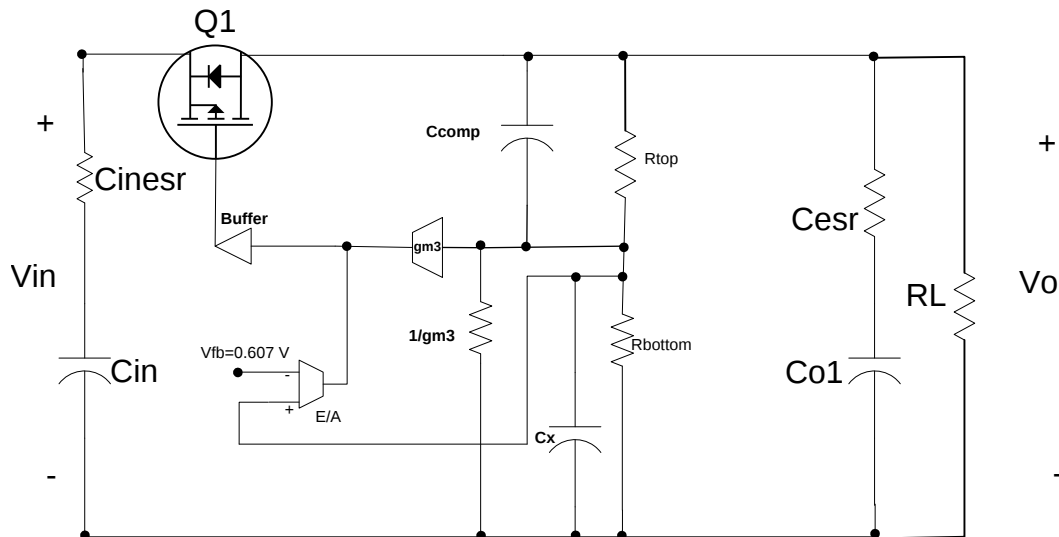


Figure 22. TPS7H1101-SP Compensation

Resistor divider composed of R_{top} and R_{bottom} determine the output voltage set points as indicated by Equation 7. Output capacitor C_{OUT} introduces a pole and a zero as shown in the following.

$$F_{p_{co}} = \frac{1}{2 \cdot \pi \cdot C_o \cdot R_L} \quad (11)$$

$$F_{z_{co}} = \frac{1}{2 \cdot \pi \cdot C_o \cdot C_{esr}} \quad (12)$$

C_x introduces a pole to the feedback loop and should be selected to compensate for the output capacitor zero, $F_{z_{co}}$.

$$F_p = \frac{1}{2 \cdot \pi \cdot C_x \cdot R_{bottom}} \quad (13)$$

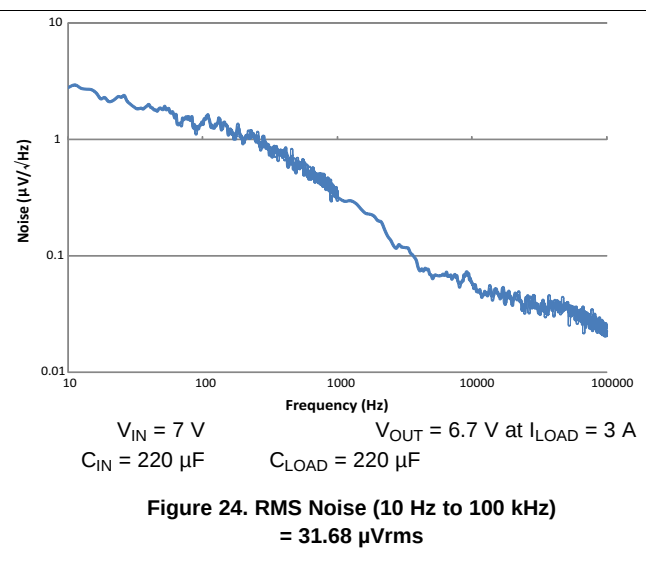
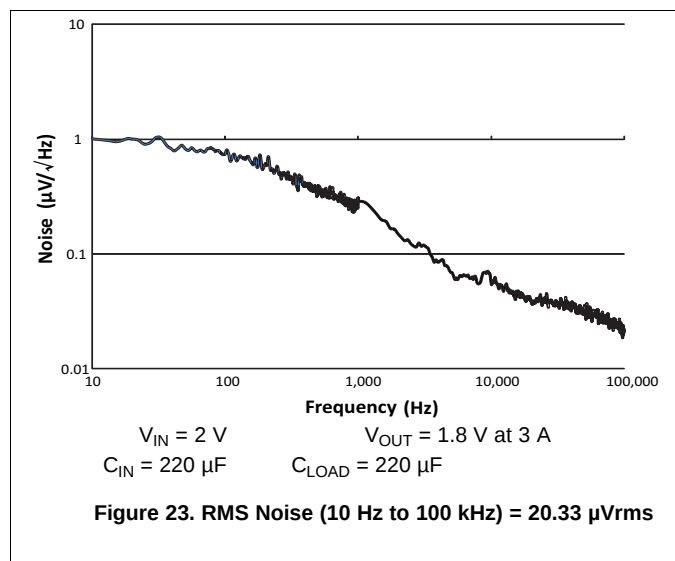
C_x is calculated to be 1000 pF for $C_o = 220 \mu F$, $C_{esr} = 45 m\Omega$.

Internal compensation in the LDO cancels the output capacitor pole introduced by C_{OUT} and R_L .

C_{comp} introduces a dominant pole at low frequency. TI recommends that a C_{comp} value of 10 nF be selected that is valid for all line and load conditions.

9.2.2.8 Output Noise

Output noise is measured using HP3495A. Figure 23, Figure 24, , and show noise of the TPS7H1101-SP in $\mu V/\sqrt{Hz}$ vs frequency.



9.2.2.9 Capacitors

TPS7H1101-SP requires the use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. [Table 3](#) highlights some of the capacitors used in the device. TI recommends to follow proper derating guidelines as recommended by the capacitor manufacturer based upon output voltage and operating temperature.

Note that polymer-based tantalum capacitors must be derated to at least 60% of rated voltage, whereas manganese oxide (MnO_2) based tantalum capacitors should be derated to 33% of rated voltage depending upon the operating temperature.

TI recommends to use a tantalum capacitor along with a 0.1- μ F ceramic capacitor for improved performance. The device is stable for input and output tantalum capacitor values of 10 to 220 μ F with the ESR range of 10 m Ω to 2 Ω . However, the dynamic performance of the device varies based on load conditions and the capacitor values used.

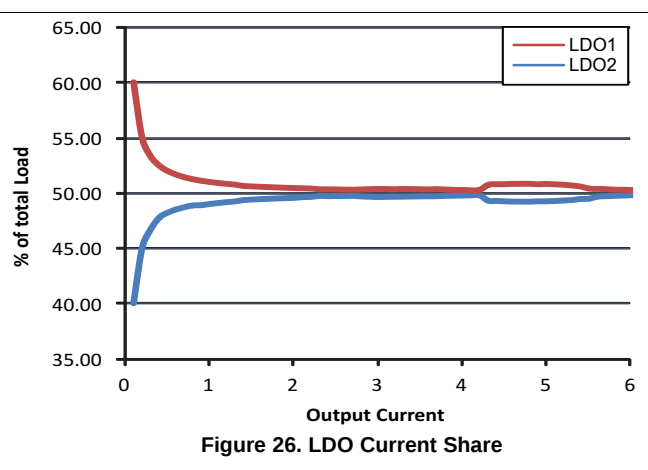
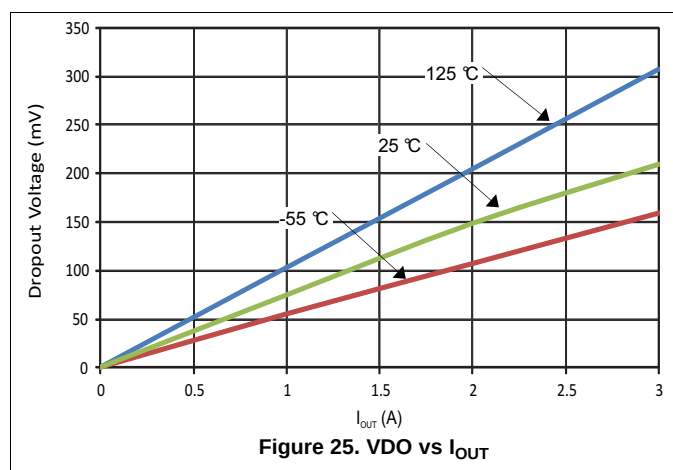
It is important to ensure that good design layout practice be followed to ensure that the traces connecting V_{IN} to GND terminals of LDO and V_{OUT} to GND terminals of LDO should be kept short to reduce inductance. Trace length should be no longer than 5 cm.

Table 3. TPS7H1101-SP Capacitors

CAPACITOR PART NUMBER	CAPACITOR DETAILS (CAPACITOR, VOLTAGE, ESR)	TYPE	VENDOR
T493X107K016CH612A ⁽¹⁾	100 μ F, 16 V, 100 m Ω	Tantalum - MnO ₂	Kemet
T493X226M025AH6x20 ⁽¹⁾	22 μ F, 25 V, 35 m Ω	Tantalum - MnO ₂	Kemet
T525D476M016ATE035 ⁽¹⁾	47 μ F, 10 V, 35 m Ω	Tantalum - Polymer	Kemet
T540D476M016AH6520 ⁽¹⁾	47 μ F, 16 V, 20 m Ω	Tantalum - Polymer	Kemet
T525D107M010ATE025 ⁽¹⁾	100 μ F, 10 V, 25 m Ω	Tantalum - Polymer	Kemet
T541X337M010AH6720 ⁽¹⁾	330 μ F, 10 V, 6 m Ω	Tantalum - Polymer	Kemet
T525D227M010ATE025 ⁽¹⁾	220 μ F, 10 V, 25 m Ω	Tantalum - Polymer	Kemet
T495X107K016ATE100 ⁽¹⁾	100 μ F, 16 V, 100 m Ω	Tantalum - MnO ₂	Kemet
CWR29FK227JTHC ⁽¹⁾	220 μ F, 10 V, 180 m Ω	Tantalum - MnO ₂	AVX
THJE107K016AJH	100 μ F, 16 V, 58 m Ω	Tantalum	AVX
THJE227K010AJH	220 μ F, 10 V, 40 m Ω	Tantalum	AVX
SMX33C336KAN360	33 μ F, 25 V	Stacked ceramic	AVX
SR2225X7R335K1P5#M123	3.3 μ F, 25 V, 10 m Ω	Ceramic	Presidio Components Inc

(1) Operating temperature is -55°C to 125°C .

9.2.3 Application Curves



10 Power Supply Recommendations

This device is designed to operate with an input voltage supply up to 7 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

- For best performance, all traces should be as short as possible.
- Use wide traces for IN, Out and GND to minimize the parasitic electrical effects.
- TI recommends a minimum output capacitor of 22 μ F with ESR of 1 Ω or less to prevent oscillations. X7R dielectrics are preferred. See [Table 3](#) for various capacitor recommendations.
- Place the output capacitors (COUT) as close as possible to the OUT pin of the device.
- Enable pin pulled up to Vin.
- Soft Start pin can be used to perform enable/ disable function as shown in [Figure 10](#).

11.2 Layout Example

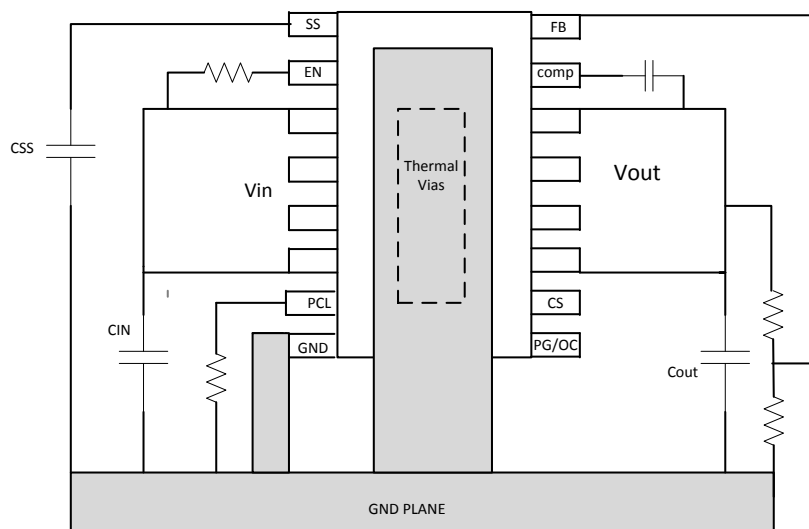


Figure 27. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

- (1) Fundamentals of Power Electronics - Robert W. Erickson, Dragan Maksimovic Ref:
- (2) An unconditional Stable linear regulator – Steve Sandler , picotest
- (3) Five things Every Engineer Should know about Bode Plots - Steve Sandler, Picotest
- (4) Evaluating Feedback Stability When there is no Test Point - Steve Sandler, Picotest.
- (5) Non-Invasively Assess your Multiple-Loop LDO's Stability – Steve Sandler, Electronic Design Jan 7, 2014.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Device Nomenclature

KGD Known good die

RHA Radiation hardness assurance for space systems

5962R13202 Same device as TPS50601-SP, shown with standard microcircuit drawing (SMD)

TPS7H1101-SP Same device as 5962R10221, shown with TI package drawing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1320201VXC	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 125	5962-1320201VXC TPS7H1101-SP	Samples
5962R1320201VXC	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 125	5962R1320201VXC TPS7H1101-RHA	Samples
TPS7H1101HKR/EM	ACTIVE	CFP	HKR	16		TBD	NIAU	N / A for Pkg Type	25 Only	TPS7H1101HKREM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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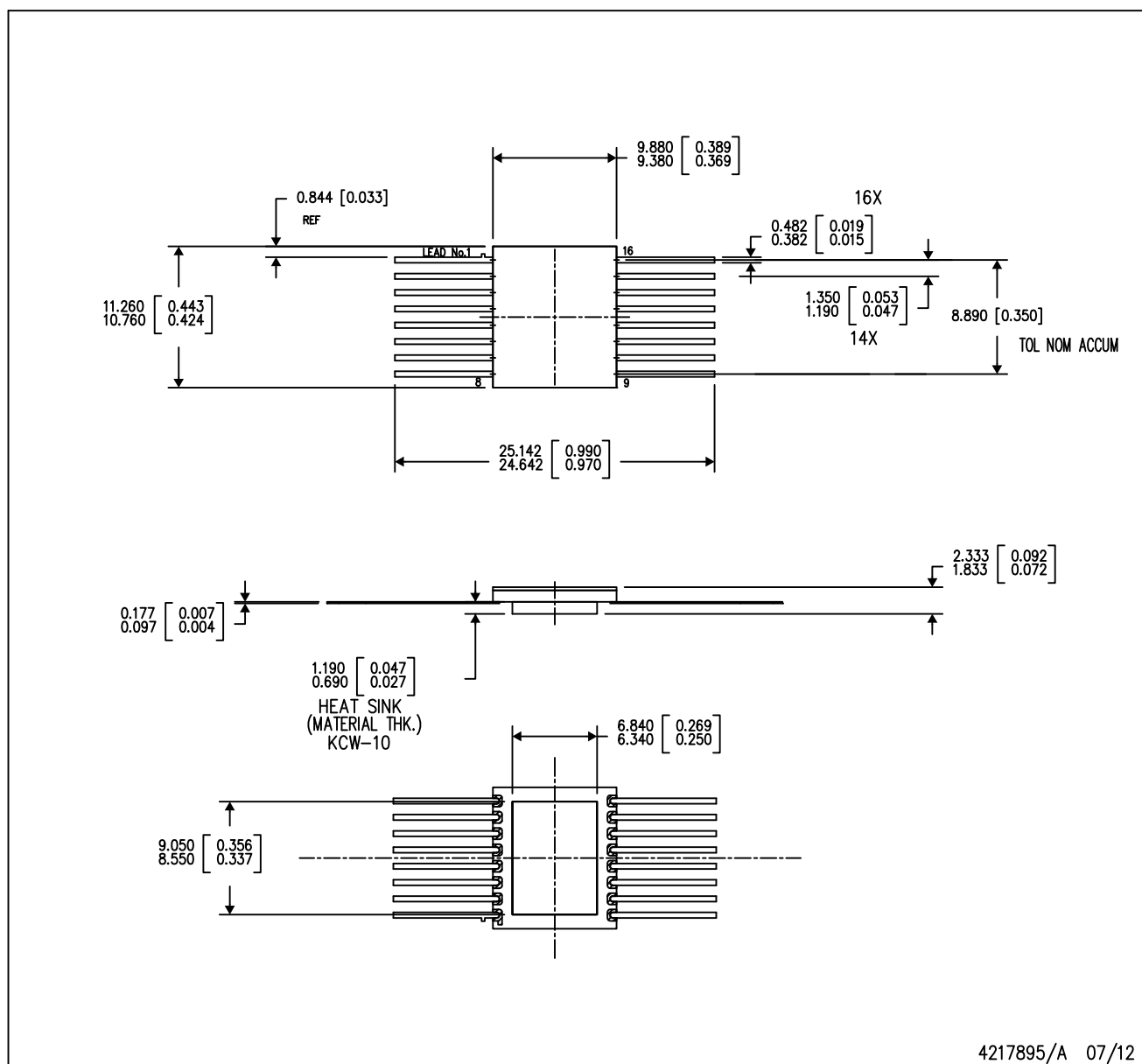
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MECHANICAL DATA

HKR (R-CDFP-F16)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in millimeters (inches).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid. Lid and heat slug are connected to pin 8 (Gnd).
- D. The terminals will be gold plated.

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